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PCB TESTER SELECTION FOR FUTURE SYSTEMS

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**Rome Laboratory
Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700**

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RL-TR-92-162, Vol I (of two) has been reviewed and is approved for publication.

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EXECUTIVE SUMMARY

The Air Force's experience has been that printed circuit board (PCB) tester acquisition is a major cost driver associated with virtually every acquisition program. Without proper planning, the PCB tester acquisition can result in program cost overruns. PCB acquisition planning is made difficult by the fact that tester needs are not fully definable until the acquisition program contract has been signed. Also, maintenance policies with respect to throwaway versus repair can change, creating a need for test equipment that was unplanned and undefined. An additional difficulty is that, over the years, capabilities and technology of avionic equipment development process could not adequately address the maintenance of the new equipment at initiation or deployment.

The main product of this effort discussed in this volume is the software which can be used to assist in the selection of printed circuit board (PCB) tester or testers for an electronic PCB. The inputs are the parameters on the PCB that need to be measured, and their ranges; and a database of PCB testers from which to choose. A limited database is provided with the software. The output is one of a selection of reports on the suitability of the testers selected from the database to test the PCB whose parameters were entered.

This software is available in two versions which have different databases. The first version is available to both U.S. Government agencies and qualified Government contractors. The second version contains proprietary data in the database and is available only to U.S. Government agencies. Availability of the software is discussed in Section 3.6. Both the software and the User's Manual have been placed in the Defense Technical Information Center (DTIC).

Adding the desired testers to the database is relatively easy. While deleting testers is not very easy, the testers to be considered in any given situation may be selected easily.

A survey was made of current and planned PCB testers and the parameters and range of those parameters which those testers can measure. In addition, a survey was made of the technology used, or expected to be used, in current PCBs and those expected to come on line within 4 to 6 years. The output of that survey was the parameters and range of parameters which AF PCB testers will need to be able to measure within the next 4 to 6 years. From the output of these surveys, a specification discussed in this volume was written defining a limited family of testers to cover the gaps between the capability of existing and planned testers and the requirements of existing and planned AF PCBs.

The details and results of the survey of AF PCB Technology are given in Volume 2. Basically, this consists of lists of the ranges of values required for the parameters in current and expected systems. Projections are made for some of these parameters as a function of time. Initially Volume 2 is being given a very limited distribution. Volume 2 has been placed in DTIC for those needing a copy.

1.0 INTRODUCTION

1.1 OBJECTIVE

This effort developed software to perform matching of PCB parametric test requirements with PCB tester capabilities. This was performed to select or identify test compatible PCB testers and develop a specification for a PCB tester or limited family of PCB testers which will fill the gap between Air Force tester needs and the testers expected to be available in the next 4 to 6 years. The data needed to determine what the specification should be, and to determine the PCB tester inputs which are needed by the software was provided by a survey of military and commercial PCB technology and PCB testers. The survey results are in Volume 2 of this technical report.

1.2 BACKGROUND

Over the years, capabilities and technology of Air Force avionic equipment have advanced rapidly in sophistication. In the past, this avionic equipment development process did not adequately address the maintenance of this new sophisticated equipment at the time of deployment. Consequently, lack of design for testability and inadequately equipped depots and other maintenance echelons were responsible for driving up maintenance costs.

Thus, a need to determine easily and quickly the availability of compatible PCB testers (i.e., ATE) to satisfy new PCB test requirements in a cost-effective way was recognized. This cost-effectiveness was to be based on such factors as price, operational requirements, training needs, size, and availability in Air Force inventory.

1.3 METHODOLOGY

This effort began with a survey of data sources from both the commercial and military domain to provide the most recent PCB technology and knowledge. Since advanced military technology and performance capabilities are often classified or otherwise unobtainable, advanced commercial technology was used as a guide for state-of-the-art technology and performance capabilities. We visited Government and industrial installations and mailed survey forms to members of the Modular Automatic Test Equipment (MATE) User's Group. The resulting data was organized and analyzed.

The data were used to determine the difference (technological void) between the test parameters which current and planned testers will measure and the test parameters which the AF PCB of the next 4 to 6 years will require to be measured. This was used to write a specification for PCB tester, or a limited family of testers, which would be expected to be able to fill this technological void. This is covered in Chapter 2.0 and the details of the specification are in Appendix A.

A prime objective of this effort was to build a computer program which would aid in the selection of a PCB tester given the characteristics of a PCB. The data collected tells us what parameters PCB testers normally measure, and what parameters need to be measured. Using this information and a commercial database, we built a program to run on an IBM compatible PC which will provide a report on the suitability of the testers selected to test a given board. The program contains a limited database of PCB testers, and more may be easily added. The user may select any or all of the testers in the database for comparison with the needs of the PCB. This is discussed in Chapter 3.

2.0 PCB TESTER REQUIREMENTS PROJECTIONS

2.1 INTRODUCTION

This section discusses the stimulus and measurement test equipment capabilities projected to be required for support of current and future Air Force Avionic systems in the next four to six years, which was used to specify in Appendix A a limited family of testers to fill the expected gap in testers between what would be needed and what would be expected to be available. Component technology changes (e.g., VHSIC, MIMIC, optical-electronics, ASIC) in this time frame will have a profound effect upon Air Force Avionic equipment design, rendering most existing or near-term planned military ATE systems obsolete. Also, any future test requirements for PCB testers will be impacted by design for testability features (e.g., Built-In-Test Equipment, critical test points, embedded self-test software) incorporated into the Air Force avionic equipment of the future.

2.2 TEST REQUIREMENTS

2.2.1 GENERAL

In general, the Air Force PCB tester requirements involve the cost-effective use of off-the-shelf ATE systems and rack-and-stack instrumentation, while committing to downsizing and standardization (e.g., full implementation of the VXI bus standard) of this instrumentation. This will require the Air Force to seek out and certify ATE PCB testers and instrumentation, both rack-and-stack and VXI, that can satisfy current and future Air Force Avionic equipment test requirements, standardization, and downsizing needs.

However, there is a major Air Force ATE system standards requirement that affects the implementation of the above solution. It is the Air Force MATE CIIL interface requirement for Air Force ATE instruments. Unfortunately, the existing CIIL instrument inventory does not include all the required instruments which would fill the technology testing gap existing between present PCB testers and PCB testers expected to be available in the next 4 to 6 years.

2.2.2 ANALOG TESTING

According to the industry survey, the analog technology drivers that are presently having the greatest immediate impact in creating testing technology voids on existing military PCB testers are mixed-signal devices, VSHIC, MIMIC and ASIC components, fiber optics, optical electronics systems, spread spectrum systems, and video signal/display systems.

The challenges facing the mixed-signal device testing are readily apparent in two emerging technologies: high-speed communications devices such as Integrated Services Digital Networks (ISDNs), Local Area Networks (LANs), modems; and next-generation video-processor devices. Each of these technologies requires specialized test techniques and hardware designed to function within the overall mixed-signal tester architecture.

The characteristics of traditional mixed-signal testing are fairly straightforward; data appears in analog form on one side of a device and in encoded or digital format on the other. But, the data in the traditional case are still analog. Thus, all that is required for testing are waveform synthesizers and digitizers to perform the data conversion from software to the real world and back again.

Testing of newer mixed-signal devices, such as data communication devices, however, is fundamentally different. The purpose of this type of device is to move binary data from one place to another, not to transfer analog signals. In this sense, testing a data communication device is more akin to testing a purely digital device; a digital input causes an expected digital output. However, to complicate the matter, one of the signals is not binary, but rather is analog encoded. The data manipulation algorithms become too complex to be handled by software data generation. Therefore, there is a need for specialized data communication test instruments that produce the required waveforms and analyze the signals. Such instruments work in real time, producing the encoded and correct data stream to the mixed-signal device while coordinating and synchronizing the analog and digital test functions.

From the VHSIC, MIMIC, and ASIC components development programs will emerge large scale analog ICs and a demand for hybrid and surface-mounted chips that will drive up the complexity of analog testing and present new challenges to the testing community. These challenges will be brought about by the complex nature of these new chips which is due to their high density, surface-mounting, and mixed-signal test requirements. All of this adds up to denser and more complex mixed-signal PCB's with possibly few test points for fault diagnostics. Consequently, analog testing will require using software aids such as hybrid circuit simulators, artificial intelligence techniques or analytic algorithms rather than just performing simple analog parameter measurements and providing analog stimulus.

The testing needs of fiber optics and optical electrical systems are similar to those of data communications devices, in that they require specialized optical test instruments because of the optical interface requirements and specialized stimulus and measurement testing techniques.

Next generation video-processors will have today's peripheral component functions integrated on one IC. They will thus contain all color and brightness signal processing functions, horizontal and vertical synchronizing functions, dynamic gray-scale correction, pincushion and corner raster-correction circuitry. There possibly may be multi-standard interfaces as well. All functions will be controlled by a general-purpose digital bus. There will be no dc voltage control lines. All adjustments will be made through embedded D/A converters addressed via the digital bus. The test of such a device is very complex, requiring perhaps 200 tests and over 3000 measurements for each device. Therefore, using traditional RAM video for the source and RAM memory for pattern storage will require too much test time. Specialized video test signal generation and video test signal analysis will be required to test this technology cost effectively.

Future Air Force systems and the current Air Force Avionic systems, which will be around for many years to come, will require the common core of analog test equipment which are available in common PCB testers. This common core of test equipment is listed below:

- o Stimulus instruments
 - Arbitrary Waveform Generator
 - Pulse Generator
 - DC & AC Power Supplies

- o Measurement instruments
 - Digital Multimeter
 - Frequency Counter/Timer Interval
 - Digitizer

Any limited family of PCB testers (reference Appendix A), should include the test instruments identified above with performance capabilities that meet the test needs of Air Force Avionic equipment for the next four to six years.

2.2.3 DIGITAL TESTING

According to the technical survey, the area of digital testing capability of military PCB testers is the most crucial technology testing void. The current military testers have an effective test rate that is too slow to cost effectively handle even current digital testing requirements. The flexibility of the digital testing is inadequate to provide the complex timing and control signals needed to test today's or tomorrow's digital PCB's.

For years, digital technology advances have been requiring digital testing of increasingly more complex circuit boards operating at dynamically higher and higher frequencies with bus-oriented architecture. This trend will continue beyond the four to six year scope of this report. Future digital technology test requirements will become more stringent as time goes on. Thus, static digital testing for detecting stuck-at-one and stuck-at-zero faults is becoming more ineffective and obsolete, as explained below.

With the advent of dynamic VLSI (i.e., microprocessors, correlators, and DRAMS) which must be operated within a specified range of clock frequencies in order to function properly, digital stimulus and measurements must be dynamic. Specified dynamic rates can be in the 1 to 100 megahertz frequency range for data and 1 to 500 megahertz frequency range for clocks in future PCB's. For handling the bus architecture PCB's, any interface between the PCB tester

and the board under test must be bi-directional and capable of switching on the fly at very high speeds to emulate the actual operational system environment for detection of dynamic or marginal faults.

Bus architecture PCB's can make traditional dynamic vector pattern testing difficult or even incompatible with the operational test requirements, because emulating the required timing between bus signals uses so many memory addresses that the actual effective signal rates are far below what is required to truly detect dynamic faults. To further compound the problem, the bus interface is often the only available access to the PCB through which it can be tested. Thus, the dynamic testing must be performed with timely and accurate signals that can emulate the bus interface, or the PCB tester must provide the bus interface required.

Required uninterrupted pattern strings are becoming longer and longer. These pattern strings are getting into the millions of patterns per second, making memory behind a pin and speed more critical than ever to test the VLSI (e.g., 64k-1Mbits RAMs or DRAMs, microprocessors, ASIC) populated PCB's, just for screen testing alone. The requirements to perform fault isolation on these complex PCB's place a need for even more patterns and more sophisticated testing and diagnostic techniques (e.g., signature analysis, in-circuit emulation, guided probe, fault dictionary, acknowledge database, artificial intelligence).

In a nutshell, test requirements for the current and near future technology are basically for a digital test system that can generate dynamic test patterns consisting of a combination of the three components described below.

- o Timing Set

The timing set length is the system clock rate. The stimulus signal edges for

logic highs and lows must be placeable within nanoseconds in the timing sets, which are also known as stimulus phases. Also, the measurement period timing edges must be placeable within nanoseconds in the timing sets, which are also known as measurement windows.

- o **Format**

The signals can be programmed to have any one of the following five formats: Non-Return to Zero, Return to Zero, Return to One, Return to Off, and Return to Complement.

- o **Data**

The data can be programmed to any given sequence of ones and zeros.

The tester should also be capable of employing combinations of test strategies such as those listed below:

- o **Simulator support for go/no-go and diagnostics test development.**
- o **Signature analysis**
- o **Guided Probe**
- o **Fault Dictionary**

2.3 BUS INTERFACES

The PCB's with bus interfaces are certainly common today and will continue in the future, with trends towards higher and higher data rates that should approach the magnitude of 1 Gbytes/s by 1996. Future buses that will accommodate these high data rates will most

certainly be optical. Since it is most likely that the Air Force will take advantage of this new technology, the number of fiber optic bus interfaces and their data rates in Air Force equipment will increase in the next four to six years. Future Air Force PCB testers must accommodate these optical bus interfaces (e.g., MIL-STD-1773 bus) and the current common data buses.

3.0 FUTURE PCB TESTER SELECTION SOFTWARE TOOL

3.1 INTRODUCTION

A future PCB tester selection computer software tool was developed to run on an IBM Compatible PC using Clarion Professional Developer™ and delivered to the Rome Laboratory (see Section 3.6) for distribution. The purpose of the software tool is to enable the user to input test requirements of a particular PCB on an IBM compatible computer, and match these test requirements with PCB testers to identify those testers that can test the PCB in question. This software will run on any IBM PC having 640K of available memory and 14MB of hard disk memory space to run the software.

3.2 PCB TESTER DATABASE

The PCB testers included in the database were testers found in the Air Force, Navy, and Army PCB tester inventory, and the commercial marketplace. They are listed in Appendix B. The tester parameters used by the PCB Selection Software are too extensive to be identified in this report, but they are identified in the *Software User's Manual for the Device Under Test/Automatic Test Equipment Matching Algorithm (DAMA)*.

The performance data collected on the individual testers was obtained from tester specifications which were supplied by the military for the military testers and by commercial tester vendors for commercial testers. The detailed commercial data needed in some cases was company proprietary, which makes the complete database available only to U.S. Government agencies. However, a shortened non-proprietary version was assembled for military contractor use. Our definition of commercial tester's capabilities is based upon the standard vendor tester

configuration. Thus, if any development work is required to provide a particular enhanced capability, this additional capability is not reflected in the database. The data collection revealed that commercial PCB testers go through frequent configuration changes which involve upgrading the testers' performance. These changes need to be reflected in the database by periodic updates.

3.3 PCB/ATE PARAMETERS MATCHED

The PCB/ATE parameters used by the PCB tester selection software tools are identified in the *Software User's Manual for the Device Under Test/Automatic Test Equipment Matching Algorithm (DAMA)*. These parameters were selected using MIL-STD-1345B, MIL-STD-1519, and the PCB technology parameters found in the technology survey.

3.4 REPORT GENERATOR

The following types of reports can be generated using the PCB tester matching software:

- o Functional Summary Report - This report processes and provides the associated comparison messages only for the functional data compared.
- o Functional "Fit" Report - This report processes and provides all compared functional data including all specific comparison numerical results and associated comparison messages.

- o **Basic Parametric Summary Report** - This report processes and provides the associated comparison messages only for the functional data and required parametric data compared.
- o **Basic Parametric "Fit" Report** - This report processes and provides all compared functional data and required parametric data compared including all specific comparison numerical results and associated comparison messages.
- o **Full Parametric Summary Report** - This report processes and provides the associated comparison messages only for the functional data compared and all the parametric data compared.
- o **Full Parametric "Fit" Report** - This report processes and provides all compared functional data and all parametric data compared including all specific comparison numerical results and associated messages.

3.5 SUPPORT DOCUMENTATION

The PCB Tester Selection Software Tool has two support documents: a Software User's Manual and a Software Programmer's Manual.

3.5.1 SOFTWARE USER'S MANUAL

The purpose of the Software User's Manual is to provide information necessary to successfully install and execute Device Under Test/ATE Matching Algorithm (DAMA). The

Manual is organized into seven major sections and four appendices. In addition to the first two sections which cover introductory material, the other five sections and appendices cover:

- a. **Installation and setup:** Discusses the hardware requirements, disk and directory organization, operating system and environmental considerations. Also, it describes an automatic procedure for installing the DAMA software distribution disks through a single 5.25 inch floppy disk drive where the distribution disk DAMA #1 contains the file INSTALL.EXE which is executed on drive A or B of the target PC and typing INSTALL at the DOS prompt (A: or B:) starts the install program. This section also discusses command line options for tailoring some aspects of DAMA's run-time performance.
- b. **System Overview:** Explains the organization of the DAMA software from the perspective of database and application organization. The organization of the principal databases is discussed in terms of their master files, resource/requirement lists and associated parameter files. The role of key fields in relating data from these various files is discussed. In addition to the system overview, this section also identifies PCB tester database parameters used in DAMA and describes how to fill out the data entry worksheets prior to updating either the ATE or PCB databases.
- c. **Execution Procedures:** Covers specific execution procedures, including common keystrokes used to manipulate DAMA's common application objects: menus, tables and forms. This section discusses DAMA's overall structure regarding the Menus, Tables and Forms Reference. This section also explains how to run DAMA's Report Generator. The Report Generator is the vehicle for the matching algorithm.

- d. **Error Messages:** Lists DAMA's general error handling mechanism. Errors are grouped by function. Where appropriate, the most probable errors within a group are highlighted along with possible solutions.
- e. **Notes:** Contains supplementary information about the application and a list of acronyms.
- f. **Appendix A: Menus, Tables and Forms Reference** - Appendix A contains graphic representations of all menus, tables and forms employed by DAMA. It is intended as a reference which can be consulted prior to data entry.
- g. **Appendix B: ATE Data Entry Worksheets** - Appendix B contains a set of blank data entry worksheets for ATE systems. These worksheets can be copied. These worksheets should be filled out prior to data entry. The ATE data entry worksheets are discussed in Section 4.0, System Overview.
- h. **Appendix C: PCB Data Entry Worksheets** - Appendix C contains a set of blank data entry worksheets for PCB systems. Like the ATE worksheets, these can be copied for use prior to data entry.
- i. **Appendix D: Glossary** - Appendix D contains definitions of terms used in the application and is included to augment understanding of the data required.

3.5.2 SOFTWARE PROGRAMMER'S MANUAL

The purpose of the Software Programmer's Manual (SPM) is to provide information necessary to successfully maintain and modify DAMA. To this end, the Manual is organized into five sections and ten appendices described below.

- a. **Scope:** This section is divided into the following three paragraphs.
- **Identification:** This paragraph contains the approved identification numbers, titles, and abbreviations, of the application, Computer Software Configuration Items (CSCI(s)), and the target computer(s) to which this SPM applies.
 - **System Overview:** This paragraph states the purpose of the application and the computer system(s) to which this SPM applies.
 - **Document Overview:** This paragraph summarizes the purpose and content of the manual.
 - **Document Conventions:** This paragraph identifies hardware, keyboard, and file/module referenced.
- b. **Referenced documents:** This section lists by document number and title all documents referenced in the manual. This section also identifies the source for all documents not available through normal Government stock activities.

- c. **Software Programming Environment:** This section is broken down into multiple paragraphs and subparagraphs and describes the host and target computer(s) operating system, and other software involved in loading, compiling, and executing the software.
- **Equipment configuration:** This paragraph describes the components and configuration of the host and target computer systems.
 - **Operational Information:** This paragraph identifies the programming language used, describes the environment, and identifies library routines and functions provided by the language supplier.
 - **Directory Organization:** This paragraph describes the equipment (e.g., disks, and other peripheral equipment) necessary to perform compilations and assemblies on the computer system. It also, by name and version number identifies the editor, linker, link-editor, compiler, cross-compiler, other utilities used, and appropriate reference manuals and describes their use. This paragraph highlights any special flags or instruction necessary for loading, executing, or recording the results of compilations.
- d. **Programming Information:** This section divides into multiple paragraphs and describes programming information relative to the database application.
- **Programming Features:** This paragraph describes the overall structure of the database/application. Additionally, this paragraph describes major modules and their functions.

- **Program Instructions:** This paragraph describes how the database application may be rebuilt after program modifications are made. This paragraph also describes how to re-compile and re-link the application as appropriate.
 - **Input and Output Control Programming:** This paragraph describes the input and output control programming of the database application.
 - **Additional or Special Techniques:** This paragraph describes additional or special programming techniques associated with the computer system.
 - **Programming Examples:** This paragraph provides examples that demonstrate the programming features described above.
 - **Error Handling:** This paragraph describes the error detection and diagnostic features associated with the application.
- c. **Notes:** This section contains general information that aids in understanding this document. This section includes an alphabetical listing of all acronyms, abbreviations, and their meanings as used in this document.

Appendix A through Appendix J: These appendices outline the underlying structure and associations of the software module used by the DAMA software program.

3.6 OBTAINING THE SOFTWARE

There are two versions of the DAMA software with support documentation. The first version is proprietary to some of the companies which supplied data, and may be sent only to U.S. Government agencies. The proprietary data has been removed from the other version, and it may be sent to anyone working on a U.S. Government contract, or to any U.S. Government agency.

Both versions of the DAMA software with support documentation have been placed in the Defense Technical Information Center (DTIC). U.S. Government agencies may obtain either version from DTIC, and contractors may obtain the non-proprietary version from DTIC. The following AD numbers will be needed to order products from DTIC:

DAMA Software, v1.0, 2 April 91

Non-proprietary version on 5 1/4" 1.2 M diskettes: AD-M200094

Non-proprietary version on 5 1/4" 360 k diskettes: AD-M200093

Proprietary version on 5 1/4" 1.2 M diskettes: AD-M200095

Proprietary version on 5 1/4" 360 k diskettes: AD-M200096

Software User's Manual for DAMA: AD-B162294

Software Programmer's Manual for DAMA, Volume I: AD-B162295

Software Programmer's Manual for DAMA, Volume II: AD-B162296

Software Programmer's Manual for DAMA, Volume III: AD-B162297

For both Government agencies and contractors, Rome Lab/ERSR must receive and RL/SC must approve the appropriate set of Terms and Conditions before DTIC may release the software. In addition, contractors must also send a copy of their approved DD Form 2345 to

RL/ERSR, Griffiss AFB, NY 13441-5700. Information on the DD Form 2345 may be obtained from the United States/Canada Joint Certification Office, 74 N. Washington, Battle Creek, Michigan, USA 49017-3084 or from (800) 352-3572.

For quickest results send the necessary papers to Rome Lab at about the same time you send a request to DTIC. The Terms and Conditions statements are the next four (4) pages of this report. If you have any questions, call the Project Engineer, Roy F. Stratton at (315) 330-4205 or DSN 587-4205.

Non-Proprietary Version

**STATEMENT OF TERMS AND CONDITIONS RELEASE OF AIR FORCE OWNED
OR DEVELOPED COMPUTER SOFTWARE PACKAGES**

Date: _____

1. Release of the following US Air Force software package (computer programs, systems descriptions, and documentation) is requested:

Rome Laboratory's PCB Tester Selection for Future Systems

2. The requested software package will be used for the following purpose:

Such use is projected to accrue benefit to the Government as follows:

3. I/We will be responsible for assuring that the software package received will not be used for any purpose other than shown in Paragraph 2 above; also, it will not be released to anyone without prior approval of the Air Force. Further, the release of the requested software package will not result in competition with other software packages offered by commercial firms.
4. I/We guarantee that the provided software package, or any modified version thereof, will not be published for profit or in any manner offered for sale to the Government; it will not be sold or given to any other activity or firm, without the prior written approval of the Air Force. If this software is modified or enhanced using Government fund, the Government owns the results, whether the software is the basis of, or incidental to a contract. The Government may not pay a second time for this software or the enhanced or modified version thereof. The package may be used in contract with the Government but no charge may be made for its use.
5. The US Air Force is neither liable nor responsible for maintenance, updating or correcting any errors in the software provided.
6. I/We understand that no material subject to national defense security classification or proprietary rights was intended to be released to us. I/We will report promptly the discovery of any material with such restrictions to the Air Force approving authority. I/We will follow all instructions concerning the use or return of such material in accordance with regulations applying to classified material, and will make no further study, use, or copy such material subject to security or proprietary rights marking.

7. I/We understand that the software package received is intended for domestic use only. It will not be made available to foreign Governments nor used in any contract with a foreign Government.

Signature of Requestor

Signature of Air Force
Approving Authority

Name of Requestor

Name/Title of Air Force
Approving Authority

Organization/Address

Organization/Location

City, State, and Zip Code

Proprietary Version

STATEMENT OF TERMS AND CONDITIONS RELEASE OF AIR FORCE OWNED
OR DEVELOPED COMPUTER SOFTWARE PACKAGES

Date: _____

1. Release of the following US Air Force software package (computer programs, systems descriptions, and documentation) is requested:

Rome Laboratory's PCB Tester Selection for Future Systems

2. The requested software package will be used for the following purpose:

Selection of Automatic Test Equipment (ATE) and examination of the ATE database for the following U.S. Government programs.

Such use is projected to accrue benefit to the Government as follows:

1. Save time (and hence, money) in the selection of ATE.
 2. Perform a better (more complete) comparison of ATE.
3. The requester agrees that the Rome Laboratory PCB Tester Selection for Future Systems shall not be used for any purpose other than shown in Paragraph 2 above, and will not be released to anyone without prior approval of the DoD Ordering Activity. Further, the software package shall not be used in competition with other software packages offered by commercial firms.
 4. The requester understands that much of THE DATA IN THIS PROGRAM IS PROPRIETARY to the companies that supplied it, and must be protected accordingly. Providing this program or the data herein to firms or individuals outside of the Government (including Government contractors), may subject the releaser to criminal prosecution pursuant to 18 U.S.C. 1905.
 5. The requester agrees that the Rome Laboratory PCB Tester Selection for Future Systems software, and/or modified version thereof, will not be published for profit or in any manner offered for sale to the Government; it will not be sold or given to any other activity or firm without prior DoD written approval. If this software is modified or enhanced using Government funds, the Government owns the results, whether the software is the basis of, or incidental to, a contract. The Government will not pay a second time for this software or enhanced or modified version thereof. The software package may be used in contracts with the Government but no charge may be made for its use.

6. The requester agrees that the U.S. Air Force is neither liable nor responsible for maintenance, updating, or correction of any errors in the above software package nor is the U.S. Air Force liable for any loss that may result due to current errors in the program.

7. The requester agrees that no material subject to national defense security classification was intended to be released as part of this software and will promptly report the discovery of any material with such restrictions.

8. The requester agrees that the Rome Laboratory PCB Tester Selection for Future Systems software package is intended for domestic use only. It will not be made available to foreign Governments nor used in any contract with a foreign Government.

Signature of Official
signing for Requester

Signature of Air Force
Approving Authority
(Rome Laboratory)

Name/Title of Official
signing for Requester

Name/Title of Air Force
Approving Authority

Organization/Address

Organization/Location

City, State, and Zip Code

Phone Number

4.0 CONCLUSIONS AND RECOMMENDATIONS

4.1 CONCLUSIONS

The following conclusions were reached regarding Air Force PCB technology trends and satisfaction of Air Force PCB test requirements for the next four to six years:

- a. In the 1990 through 1996 timeframe, the rate of technological progress promises to be greater than any previously experienced. In addition, the technology lag of seven to ten years between military and commercial technology should decrease due to the effort of such programs as VHSIC and MIMIC. Consequently, Air Force Avionic equipment technology will be substantially technologically advanced and more in line with contemporary industrial technology than it is today. With the VHSIC and MIMIC programs coming to completion in the 1990's, deployed military systems will experience a general increase in digital systems operating frequency of 60 to 100 MHz and bus data rates in the order of 50 to 100 Mb/s. Fiber optics will also be used more and more in systems, particularly in the area of fiber optic buses.
- b. In order to be cost-effective, the new technology involving mixed-signal devices, VSHIC, MIMIC and ASIC components, video-processors, fiber optics, and optical electronics, will require PCB testers with specialized instruments that relate directly to the function of the PCB under test.
- c. All of the Air Force hardware test requirements for the next four to six years, except for the highest speed dynamic digital formatted cycle test with data rates over 80 MHz, are currently covered by the most accurate and capable test equipment existing.

Existing test equipment includes all the commercially GPIB (IEEE-488) programmable equipment that is available and can be integrated into any GPIB expandable ATE system, whether military or commercial. However, the instrument software driver routines library would need to be developed. In other words, there is not a readily available fully-integrated family of existing PCB testers, nor are there any known planned PCB testers that presently satisfy all of the Air Force test requirements.

- d. Based on the above, it was concluded that a need exists for a top-level specification for an Air Force high-tech family of PCB testers to fill a technical void in testing future complex PCB's. A specification is provided in Appendix A. As for the low to medium complex PCB's, existing Air Force ATE inventory includes testers such as the AN/USM-465 (digital), AN/USM-385 (hybrid) and others that appear to meet the need.
- e. For some programs a cost-effective alternative solution to a highly expensive military ATE system may be a commercial PCB tester. In fact, a family of Air Force pre-approved IEEE-488 bus expandable commercial ATE PCB testers may be appropriate. Such a family of testers would have to include some high-tech hybrid ATE to test complex PCB's and low or medium end ATE to test PCB's that fall into one of the following categories: low volume, low cost, simple to medium complexity, or in need of field support. This family of testers would have to include such commercial ATE systems as are identified in Appendix C, or equivalent or better performing ATE which were not identified during the survey.
- f. It is much easier to upgrade the Air Force's inventory of analog ATE than its digital ATE. The state-of-the-art for digital testing has changed so much over the last few years that the current inventory of military PCB testers and digital word generators

does not satisfy the dynamic formatted cycle test requirements of current microprocessor digital PCB's regarding speed, timing, and software aids such as simulators. Thus, a cost-effective approach may be to look at existing commercial PCB testers with dynamic formatted cycle test capability for their digital test system's adaptability to becoming a generic digital word generator. This could satisfy the digital testing upgrading of Air Force inventory PCB testers.

- g. New testers are being continuously introduced to the commercial market with tester performance continuously improving as companies work to meet competition. For the tester database to be complete and accurate, the tester industry needs to be continuously monitored and new testers need to be added to the existing database. Otherwise the database becomes obsolete in about six months.
- h. Based on technology trends, it can be expected that new technology parameters will need to be added to the data fields of the tester database in the near future.

4.2 RECOMMENDATIONS

In order to provide some guidance to the Air Force for satisfying future test requirements, the following recommendations are made:

- a. Perform, on a periodic basis, data collection and test requirement analysis of the Air Force's latest avionic equipment and provide technical reports on technology trends and test requirements.

- b. From available test instrument technology, integrate and certify a new ATE family of military PCB tester configurations that are technologically focused and meet, as a minimum, the hardware performance and software requirements described in the specification in Appendix A.
- c. As a cost-effective alternative to the above recommendation, certify a family of commercial PCB testers (reference Appendix C) with the necessary GPIB-controllable rack-and-stack instruments and/or VXI test instruments with CIIL compatibility that meet, as a minimum, the hardware performance requirements described in Appendix A. The fact that they are listed in Appendix C does not constitute an endorsement of these testers. The sole purpose of Appendix C is to identify possible tester candidates that the Air Force may consider for certification. Such an endorsement would be beyond the scope of this report. This list should not be considered complete; other qualified testers may exist. If the CIIL requirement prevents the existing test equipment from meeting the test requirements, it is recommended that the Air Force either fund test instrument vendors to provide CIIL compatibility needed to fill the technology void or waive the CIIL requirement.
- d. Develop a generic military dynamic cycle test Digital Word Generator (DWG) with a 100 MHz data rate. The digital testing capabilities of existing Air Force inventory ATE can thus be upgraded to meet current and near term digital test requirements of Air Force PCB's. However, based on this survey, modifying an existing dynamic cycle test 20 MHz (or better) data rate DWG to fit into Air Force ATE systems would be sufficient to satisfy the large majority of the digital test requirements.

- e. Identify and certify a family of test instruments that will be focused on such technological areas as data communications, video signals, optical signals, and frequency hopping. This family of instruments should be used for technology insertion into PCB testers.
- f. Training and maintenance funding be provided to maintain the DAMA Software Database to keep both current and valid.

APPENDIX A

SPECIFICATION FOR MILITARY LIMITED FAMILY OF PCB TESTERS

1.0 INTRODUCTION

This appendix, based upon the technical survey conducted, provides top-level projected hardware function specifications for a military family of PCB's testers to support the testing of Air Force PCB technology that is currently fielded and forecasted for the next 4 to 6 years. As concluded in paragraph 4.1.b on page 4-1 the most accurate test instruments existing today can satisfy hardware requirements described below except for the high speed dynamic digital testing requirements.

This appendix specification is not formatted per MIL-STD's. The data should be taken from this appendix and placed in the appropriate documents in the format required for acquisition if and when required.

2.0 HARDWARE REQUIREMENTS

2.1 GENERAL

These hardware requirements for a member of the family of PCB testers are configured according to the major types of PCB technology listed below for which they are expected to provide testing support:

- o Hybrid (Basic analog and digital configuration)
- o RF/Microwave

- o Communication, Identification, and Navigation
- o Video
- o Electrical-Optical

These five independent configurations are needed to keep the size of a test station to a practical limit for the cabling lengths, to preserve interface performance integrity, and to allow limiting the testing assets for a particular PCB technology (i.e., RF, video, etc.).

In addition, each member of the PCB tester family will require a basic analog and digital test instrument configuration which is the Hybrid PCB tester below in order to adequately handle the testing of any major PCB technology.

2.2 HYBRID PCB TESTER CONFIGURATION

2.2.1 Controller

The controller needed for the PCB tester is a computer with at least 16 Mbytes of memory and 380 Mbyte Disk.

2.2.2 User Interface

The user interface, as a minimum, should consist of a display, keyboard, and printer.

2.2.3 General Purpose Interface

The general purpose interface must be compatible with the MATE Interface Configuration Assembly Specification excluding the digital test system I/O.

2.2.4 Test Equipment

The functional performance specifications for the essential test equipment needed in all PCB testers is as follows:

o Power Supplies

- DC power
 - 5-Programmable 0 to 30V @ 10A
 - 1-Programmable 0 to 100V @ 8A
 - 2-Programmable 0 to 500V @ 3A
- Precision DC voltage
 - 1-Programmable 0 to $\pm 100V \pm 1mV @ .1A$
- Precision AC voltage
 - 1-Programmable 0 to 200mA $\pm 1mA$
- AC power
 - 2-Programmable 0 to 250 Vrms @ 10A, 55 to 1200 Hz single phase/three (3) phase

o Digital Multimeter

- DC Volts: 0 to 1,000V
- AC Volts: 0 to 1,000V

- DC/AC current: 0 to 3A
- Resistance: 0 to 20 Megohms

- o Frequency/Time Interval Counter
 - Frequency: 0 to 100 MHz
 - Time Interval: 1ns to 100 sec
 - Events: 0 to 99999

- o Pulse Generator
 - Frequency: 0 to 200 MHz
 - Period: 5ns to 1,000msec
 - Width: 2.5ns to 1,000msec
 - Amplitude: $\pm 30V$ into 50 ohm load

- o Arbitrary Waveform Generators
 - Frequency: 0 to 25 MHz
 - Amplitude: 10mVP-P to 30VP-P into 50 ohm load

- o Signal Generator
 - Frequency: 0.1 to 50 MHz
 - Amplitude: +13 dBm to -127 dBm into 50 ohm load

- o Digitizer
 - Frequency: 0 to 200 MHz
 - 10 bit accuracy

o Loads

- 1 to 10 Kohms at 5 Watts

o Digital Test System

- I/O 256 to 1024 bi-directional dynamic pins & Short Circuit Protected
Bi-directional lines switchable on the fly on pattern by pattern and pin
by pin basis.

Stimulus/Response Logic Level: -15V to +15V

Level Resolution: $\pm 10\text{mV}$

Sink/Source Current: 75 ma.

Data Formats: RZ, NR, R1, R0, & RC

Dynamic Cycle Test Pins Group 1 (Up to 432 Pins)

Data Skew: $\pm 1\text{ns}$

Slew Rates: .25ns/volt

Formatted Cycle Data Rate: 100 b/s to 100 Mb/s

Dynamic Cycle Test Pins Group 2

Data Skew: $\pm 5\text{ns}$

Slew Rates: .25ns/volt

Formatted Cycle Data Rate: 100 b/s to 40 Mb/s

Effective Test Rate of at least 10,000 pattern/sec

Provide at least five simultaneous logic levels across the 1024 pins

Threshold level adjustable/determined in groups no larger than 36

Each pin must be under/over voltage protected

- Thirty-two Static I/O bi-directional Pins; Short Circuit Protected
voltage level -30V to +30V individually programmable
under/over voltage protected

sink/source currents max 75 ma.

- Create typical digital patterns via algorithms as listed below:

WALKING ONE & ZERO

CHECKERBOARD READ/WRITE

MARCH II

PING PONG

GALPAT

MOVI

- Perform pattern search
- Perform hand-shaking
- Perform pattern/bit masking
- Perform Signature Analysis and/or Cyclic Redundancy Check
- Pattern burst lengths up at least 64,000 @ max. data rate
- Clocks: external up to 100MHz
internal 100 to 100MHZ
- External Sync capability for start of test or pattern burst sync
- Threshold errors detection

o Guided Digital Probe

- Frequency: 0 to 40 MHz
- Capture up to 20 signal states

o Current Probe Capable

- 1 μ A to 1 Amp

o Bus Interfaces

- 2 - MIL-STD-1553 A/B

- 1 - RS-232C

Programmable baud rate: 50 to 19200

- 1 - RS-422A

Programmable baud rate: 300 to 38400

- 1 - RS-485

- 1 - IEEE-488

- 1 - Ethernet (IEEE-STD-802.3)

- 1 - MIL-STD-1397

- 2 - MIL-STD-1773 (Fiber Optic)

Frequency: 10MHz to 100 MHz high speed

In addition, all of the above test instruments must handle CIIL's standard statements, unless a waiver can be obtained for the Air Force MATE CIIL requirement, and have external sync capabilities for synchronizing system analog and digital stimulus and measurement test instruments for performing any given test.

2.2.5 Software

The PCB Tester programming language must be ATLAS or Ada, and the software capabilities below must be provided:

- o Translate files from a digital simulator (e.g., HITS or LASER) to a format usable by the PCB tester**
- o Pattern length limited by total disc storage capability**

- o Process and display threshold errors
- o Perform fault dictionary analysis
- o Store and compare measured response patterns with expected pattern response
- o Perform fault signature analysis to include:
 - Signature storage
 - Perform comparison against learned signatures
 - Display the fault set
- o Perform multiple digital test
- o Pass pattern or bit failure data to ATLAS or Ada test language
- o Perform calibration, certification and self-test
- o Digital Test System TPS integration aids:
 - Single stepping
 - Stop on fail
 - Pattern looping
 - Pattern rerun
 - Pattern modification
 - Burst rate modification
 - Failure data reporting
 - Stimulus/Response status reporting
 - Data format and display selection

2.3 RF/MICROWAVE STATION CONFIGURATION

2.3.1 CONTROLLER

The same as the Hybrid Test Station.

2.3.2 User Interface

The same as the Hybrid Test Station.

2.3.3 General Purpose Interface

The same as the Hybrid Test Station.

2.3.4 Test Instruments

This Test Station Configuration incorporates all of the test instruments of the Hybrid Test Station plus the following additional test instruments described below:

- o RF Stimulus Generator**
Frequency: 10 MHz to 40 GHz (expandable to 110 GHz)
Amplitude: +20 dBm to -110 dBm into 50 ohms
Modulation: AM/FM/PM
- o Network Analyzer**
Frequency: 10 MHz to 40 GHz (expandable to 110 GHz)
- o Spectrum Analyzer**
Frequency: 100 Hz to 22 GHz (expandable to 325 GHz)
Fundamental Amplitude: +30 dBm to -12 dBm

- o **RF Power Meter**

Frequency: 100 KHz to 40 GHz

Amplitude: -70 dBm to +44 dBm

- o **Synchro/Resolver Simulator**

Reference Input:

Frequency: 47 Hz to 10 kHz

Voltage: 2 to 115 Vrms (Programmable)

Angular Range: 0 to 359.999 degrees

Tracking Rate: 0.001 to 1000 deg/sec (Programmable)

Signal Output:

Frequency: 47 Hz to 10 kHz

Line-to-Line Voltage: 2 to 90 Vrms (Programmable)

- o **Synchro/Resolver Indicator**

Reference Input:

Frequency: 47 Hz to 10 kHz

Voltage: 2 to 115 Vrms (Programmable)

Angular Range: 0 to 359.999 degrees

Tracking Rate: 0 to 720 deg/sec

Signal Input:

Frequency: 47 Hz to 10 kHz

Line-to-Line Voltage: 2 to 90 Vrms (Programmable)

2.4 COMMUNICATION, IDENTIFICATION, AND NAVIGATION

2.4.1 Controller

The same as the Hybrid Test Station.

2.4.2 User Interface

The same as the Hybrid Test Station.

2.4.3 General Purpose Interface

The same as the Hybrid Test Station.

2.4.4 Test Instruments

This test station configuration incorporates all of the test instruments of the hybrid test station plus the following additional test instruments described below:

- o RF Stimulus Generator**

Frequency: 10 MHz to 40 GHz (expandable to 110 GHz)

Amplitude: +20 dBm to -110 dBm into 50 ohms

Modulation: AM/FM/PM

- o Network Analyzer**

Frequency: 10 MHz to 40 GHz (expandable to 110 GHz)

- o Spectrum Analyzer**

Frequency: 100 Hz to 22 GHz (expandable to 325 GHz)

Fundamental Amplitude: +30 dBm to -12 dBm
- o Synchro/Resolver Stimulator**

Reference Input:

Frequency: 47 Hz to 10 kHz

Voltage: 2 to 115 Vrms (Programmable)

Angular Range: 0 to 359.999 Degrees

Tracking Rate: 0.001 to 1000 deg/sec (Programmable)

Signal Output:

Frequency: 47 Hz to 10 kHz

Line-to-Line Voltage: 2 to 115 Vrms (Programmable)
- o Synchro/Resolver Indicator**

Reference Input:

Frequency: 47 Hz to 10 kHz

Voltage: 2 to 115 Vrms (Programmable)

Angular Range: 0 to 359.999 degrees

Tracking Rate: 0 to 720 deg/sec

Signal Input:

Frequency: 47 Hz to 10 kHz

Line-to-Line Voltage: 2 to 90 Vrms (Programmable)
- o Switching Synthesizer**

Sweep Frequency Range: 10 MHz to 18.5 GHz min.

Hopping Rate: 0 to 1 MHops/sec min.

Modulation: AM and FM

o Spread Spectrum Modulators and Demodulators Unit

Modulation types: FSK, PHASE CCSK, GPS QPSK/BPSK, and MSK

2.5 VIDEO TEST STATION

2.5.1 Controller

The controller is the same as the Hybrid Test Station.

2.5.2 User Interface

The user interface is the same as the Hybrid Test Station.

2.5.3 General Purpose Interface

The general purpose interface is same as the Hybrid Test Station.

2.5.4 Test Instruments

This test station configuration incorporates all the test instruments of the Hybrid Test Station plus the following additional test instruments described below:

- o Digital Test System**

Same capabilities as Hybrid Tester Station Digital Test Station except the formatted Cycle Date Rate is increased form 100 Mb/s to 200 Mb/s for Dynamic cycle test Pins Group 1.
- o Video Noise Meter**

Frequency: 0 to 10 MHz

Amplitude: -65 dBm to -27 dBm
- o Video Sweep Generator**

Frequency: 100 kHz to 10 MHz
- o Video Sync/Test Signal Generator**

Standards: SVHS, R-Y/B-Y and RGB
- o RGB VIDEO Generator**

Frequency Bandwidth: up to 125 MHz

Amplitude: 1 Vp-p into 75 ohms
- o Video Waveform Monitor/Vector Analyzer**

Frequency: 25 Hz to 8 MHz

2.6 ELECTRICAL-OPTICAL PCB TEST STATION

2.6.1 Controller

The controller is the same as the Hybrid Test Station.

2.6.2 User Interface

The user interface is the same as the Hybrid Test Station.

2.6.4 General Purpose Interface

The general purpose interface is the same as the Hybrid Test Station.

2.6.4 Test Instruments

This test station configuration incorporates all of the test instruments of the Hybrid Test Station plus the following additional test instruments performance capabilities described below. However, because of lack of sufficient military optical equipment technical data obtained from the survey, these performance requirements are based partially on similar commercial industry equipment test requirements.

- o Optical Pulse Power Meter**

Wavelength: 550nm to 1725nm (can be discrete sources)

Measurement Type: Peak and Average Power

Minimum Measurement Range: +0dBm to -50dBm

- o **Optical Sources**

Wavelengths (min.): 850nm, 1300nm, and 1550nm

External Modulation: 0 to 850 MHz

Output Power: -23dBm (min.)

- o **Optical Attenuators**

Wavelength: 600nm to 1650nm

Attenuation Range: 0 to 60dB

Resolution: 0.01dB

- o **Optical Signal Analyzer**

Wavelength: 825nm to 1600nm

Intensity Modulation Detection Bandwidth: 100 kHz to 22 GHz

APPENDIX B

PCB TESTER DATABASE

- o ALCC MIDATS**
- o ARTISCAN 7000+**
- o BT 3400**
- o CAT IIID (WEAPON SYSTEM)**
- o CIRCUIT CARD TESTER**
- o CTS II - CONTACT TEST SET II**
- o DATSA**
- o DTS-70 DIGITAL TEST STATION**
- o Fluke 3050B**
- o GEC AVIONICS ORION**
- o GEC AVIONICS TEST STATION**
- o HP 3070**
- o HP 75000 (VXI)**
- o IFTE - INTERMEDIATE FORWARD TEST EQUIPMENT**
- o MAATS 390 (MODULAR AVIONICS TEST STATION)**
- o MIDATA 510**
- o MIDATS part number 60585-40002**
- o OTH-B/GATS**
- o SCHLUMBERGER SYSTEM 725**
- o SCHLUMBERGER SYSTEM 790**
- o TERADYNE L293**
- o TERADYNE L393**
- o TRANSPORTABLE ANALOG TESTER (TAT)**
- o WK 950**

NOTE: An additional fourteen (14) testers are found in the Government proprietary version.

APPENDIX C

CLASSIFICATION OF FAMILY OF COMMERCIAL PCB TESTERS

- o High-End Performance Hybrid PCB Functional Testing ATE Family Examples**
 - GenRad 2750**
 - Hewlett Packard 3070**
 - Teradyne L393**
 - Schrumberger S790**
- o Medium Performance Hybrid PCB Functional Testing ATE Family Example**
 - Harris TAT**
- o Low-End Performance Hybrid PCB Functional Testing ATE Family Example**
 - HP75000**
 - Sanders Circuit Board Tester**
- o Low-End Performances Digital PCB Functional Testing ATE Family Example**
 - GenRad 2225 or 2235**

APPENDIX D

GLOSSARY OF TERMS

- A -

Access Time - A time interval that is characteristic of a storage device and is essentially a measure of the time required to communicate with that device.

Algorithm - A finite set of well-defined rules which gives a sequence of operations for performing a specific task.

Amplitude - The distance between high or low points of a waveform or signal.

Amplitude Modulation - A method of adding information to an electronic signal where the amplitude of the wave is changed to convey the added information.

Attenuator - A device that reduces the output power relative to the input power, by any means, including absorption and reflection.

Average Power - The time average of the instantaneous power over one period of the wave.

-B-

Bandwidth - The difference, expressed in Hz, (i.e., cycle per second), between the highest and lowest frequencies of a transmission channel. Bandwidth varies with the type and method of transmission. The bandwidth is the range of frequencies that can pass through a given circuit. Generally, the greater the bandwidth, the more information that can be sent through the circuit in a given amount of time.

Baud - A unit of signaling speed equal to the number of discrete conditions or signal events per second, or the reciprocal of the time of the shortest signal element in a character.

Bay - An equipment rack which is used to stack test instruments.

Bidirectional Bus or Pin - A bus or pin used by any individual device for two-way transmission of data, that is, both input and output.

Burst - A wave or waveform composed of a pulse train or repetitive waveform that starts, has a prescribed time and/or amplitude, continues for a relative short duration and/or number of cycles, and upon completion returns to the starting amplitude.

Bus - A set of signal lines used by an interface system, to which a number of devices are connected, and over which information is transferred between the devices.

Byte - A binary bit string, usually eight bits long, that is operated on as a unit and is capable of holding one character in the local character set.

-C-

Carrier - A wave having at least one characteristic that may be varied from a known reference value by modulation.

Coupling Impedance - The impedance introduced by test instruments upon being connected to the device under test.

-D-

Data Format - This pertains to how a logic one is represented during data transmission (e.g., return to zero, return to one, etc.)

Data Skew - In parallel data transmission, the difference in arrival time of bits transmitted at the same time.

Dead Time - The time after a triggering pulse during which the system is unable to be retriggered.

Delay Time - The interval of time between a specified point on the input signal and a specified point on the related output signal.

Demodulation - The process of separating a data (digital or analog) signal from an analog carrier signal.

DIF - This pertains to differential mode logic which is a family of logic utilizing the relative polarity of two input lines to specify logic status.

Digital Signal - A signal that is either zero (off) or one (on) (or one "something") rather than as a continuum of voltages.

Direct Current (DC) Offset - A direct current level that may be added to an alternating current signal.

Distortion - An undesired change in waveform.

Duty Cycle - The ratio in percent of the active or "on" time within a specified period to the duration of the specified period.

Dynamic Test - A test of one or more of the signal properties or characteristics of the equipment or of any of its constituent items performed while the equipment is energized and operating at normal frequency.

-F-

Fall Time - The time interval for the pulse trailing edge to travel between 90% and 10% of pulse amplitude.

Fiber Optics - A data transmission medium consisting of transparent fibers. Light-emitting diodes and lasers send light through the fiber to a detector, which then converts the light back into electrical signals.

Formatted Digital - For usage in this report, it pertains to the Edge Placable Digital Data used in "Dynamic Board Testing" and/or "Cycle-Based Testing" test methodologies. These test methodologies are far more flexible than the traditional memory-behind-a-pin, pattern-based digital testing. By using formatted digital testing methods, the real-time performance and intricate timing of today's electronic systems can be emulated and accurately tested.

Within the Formatted Digital Testing environment, Timing Sets are defined as the overall timing structures or Timing Templates that contain detailed timing parameters. Each Timing Set can contain several different definitions for Drive Phases which describe the initial delay and the active duration of each stimulus pin. Each Timing Set can also contain several definitions for each response pin. Many Timing Sets, each containing several Drive Phase definitions and Test Windows definitions, can be defined for a single digital board and can be changed during the testing to emulate the actual real-time operation of the board. Finally, the format in which the data is presented can be selected as Non Return, Return to Zero, Return to 1, Return to Hi-Z, and Return to Complement.

Frequency Hopping - A modulation technique used for multiple access; frequency-hopping system employ switching of the transmitted frequencies at a rate equal to or lower than the sampling rate of the information transmitted. Selection of the particular frequency to be transmitted can be made from a fixed sequence or can be selected in pseudo-random manner from a set of frequencies covering a wide bandwidth. The intended receiver would frequency-hop in the same manner as the transmitter in order to retrieve the desired information.

Frequency Modulation - Angle modulation in which the instantaneous frequency of a sine-wave is caused to depart from the carrier frequency by an amount proportional to the instantaneous value of the modulating wave. The combinations of phase and frequency modulation are commonly referred to as frequency modulation.

Frequency Shift Keying - The form of frequency modulation in which the modulating wave shifts the output frequency between or among predetermined values, and the output wave has no phase discontinuity.

-H-

Handshaking - An exchange of predetermined signals for purposes of control when a connection is established between two data sets.

Harmonic - A sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency.

Harmonic Content - The deviation from the sinusoidal form, expressed in terms of the order and magnitude of the Fourier series terms describing the wave.

Hybrid - In this usage, a piece of equipment having (or using) both digital and analog signals.

-I-

Interleave - To arrange parts of one sequence of events so that they alternate with parts of one or more other sequences of events so that each sequence retains its identity.

-M-

Man-Portable - The item is capable of being carried by one man which is usually less than 35 pounds.

Microwave - Any electromagnetic wave in the radio frequency spectrum above 1000 MHz.

Multi-Mode Fiber - A fiber that supports propagation of more than one mode of a given wavelength. This cable causes the light signal to propagate incoherently, causing dispersion effects that limit the bandwidth and distance of communication.

-N-

Nodes - Points in a network where service is provided, service is used, or communications channels are interconnected.

Noise - Unwanted disturbances superimposed upon a useful signal, which tend to interfere with the normal signal input or output characteristics.

Non-Formatted Digital - For usage in this report, this pertains to the traditional memory-behind-a-pin, pattern-based type digital data.

-O-

One-Shot - A signal which occurs once for each time it is triggered.

Optical Coupler - A junction that allows an optical power among two or more ports or concentrates optical power from two or more fibers into a single port. Couplers may be active or passive.

Optical Coupling Loss - The power loss suffered when coupling light from one optical device to another.

Optical Critical Angle - The smallest angle of incidence at which a ray may be totally reflected within at the core-cladding interface. When light propagates in a homogeneous medium or relatively high refractive index (n_1) onto an interface with a homogeneous material of lower index (n_2), the critical angle is defined by $\arcsin(n_2/n_1)$.

Optical Transmitter - A device that converts electrical signals to optical signals.

-P-

Parity - An error detection method in which the total number of ones in a binary word, byte, character, or message is set to an odd or even number by appending a redundant bit. This number is subsequently checked to ensure that it remains odd or even. Also, parity is the property of oddness or evenness possessed by a word, byte, character, or message. This property is determined by the total number of ones.

Phase - The fractional part t/P of the period P through which t has advanced relative to an arbitrary origin. *Note:* The origin is usually taken at the last previous passage through zero from the negative to the positive direction.

Phase Modulation - Angle modulation in which the angle of a carrier is caused to depart from its reference value by an amount proportional to the instantaneous value of the modulating function.

Phase-to-Phase Angle - The time, expressed in degrees, between two voltages reaching a given point on their cycle. The phase-to-phase angle is the relative phase of two signals.

Photon - A quantum of electromagnetic energy. The energy of a photon is hf where h is Plank's constant and f is the optical frequency.

Planar techniques - Formation of P or N type regions or both on a semiconductor crystal by diffusion techniques through an aperture on a protective surface layer on the crystal.

Plank's Constant - The number h that relates the energy E of a photon with the frequency g of the associated wave through the relation $E=hg$; $h=6.224 \times 10^{-34}$ joule-second.

Portable - Equipment that one man can carry which is usually required by MIL-STD's to be less than 35 lbs.

Pulse Carrier - A carrier consisting of a series of pulses.

Pulse Modulation - Modulation of one or more characteristics of a pulse carrier. The characteristics can be amplitude, pulse width, pulse position, or frequency.

-R-

Rate - The number of times an event or parameter changes or occurs per second.

Resolution - The least value between two quantities which can be detected reliably.

Ripple Voltage or Current - The alternating-current component from a direct-current power supply arising from sources within the power supply.

Rise Time - The time interval of the leading edge between the instants at which the instantaneous value first reaches the specified lower and upper 10% and 90% of pulse amplitude.

-S-

Single Mode Fiber - A fiber that allows only one mode for light because of the small core diameter of the fiber: less than 10 μm .

Static Digital - For usage in this report, this pertains to digital data that does not require or use a clock in the transfer of the input and/or output of digital data.

Surface Mounting - The electrical connection of components to the surface of a conductive pattern from without utilizing component holes.

Sweep Time - The time it takes to vary an output frequency between two selected frequency limits. It is also the time for a trace to sweep across the face of a CRT.

Slewing Rate - The maximum rate-of-change of voltage or other parameter per second at the output pin.

Synchronization rate - The rate or frequency at which the inputs and outputs of a device can be ensured to operate together in a fixed-phase relationship. The synchronization rate is the rate of the synchronization signal.

Synchro/Resolver - A device which utilizes a synchro to convert rotational position (angular data) into electrical signals (voltages). These electrical signals are proportional to the angular rotation.

-T-

Tester Envelope - This is defined to be the process of using maximum and minimum tester performance capabilities value of the equipment support tester to determine the equipment test requirements.

Three Phase Delta Configuration - The three windings are connected together and the three (incoming or outgoing) lines are connected to the three nodes.

Three Phase Wye Configuration - Three lines come to the three windings which are tied to a common point, usually a ground wire.

Tracking Rate - The rate at which a variable input quantity can be followed.

Transmission Media - Wire, coaxial cable, fiber optics, air, or vacuum, that is being used to carry an electrical signal which has information.

Transportable - An item that can be readily carried or transported from place to place.

Trigger - A pulse used to initiate action in another circuit which then functions for a period of time.

Tri-State Capability - Output buffers have three output states. Two of the output states are the common logic states 0 and 1. When the buffer is enabled by a control input, its output is either logic 0 or 1. The output impedance is low when the buffer is enabled, allowing the

output to source or sink current to the circuits it drives. The third state which exists when the buffer is disabled does not provide a conventional logic level output but, rather, causes the output to be a very high impedance. This high impedance state prevents the output from driving or loading any circuit connected to it. Thus, when disabled, three-state outputs are electrically disconnected from any logic circuits to which they are physically connected and are said to be floating.

Tri-State Switching Time - The time that is taken to switch between the three output states of the Tri-State Buffer.

-V-

Voltage Imbalance - In this usage, the difference between the highest and lowest fundamental rms (root-mean-square) phase voltage values in a three phase system.

Voltage Ripple - The alternative voltage component from a direct current power supply arising from sources within the power supply and including noise.

Voltage Tolerance - The total amount by which the output voltage level varies; thus the tolerance is the algebraic difference between the maximum and minimum voltage limits.

-W-

Wave Analysis - This pertains to the analysis performed to determine the harmonic content, distortion, rise time, fall time and amplitude etc. of a waveform.

Wavelength - The distance between two points in a periodic wave which have the same phase.

APPENDIX E

ACRONYMS AND ABBREVIATIONS

A	Ampere
A/D	Analog-to-Digital
AC	Alternating Current
Acc.	Accuracy
AEGIS	Integrated Fleet Defense System
AFB	Air Force Base
AIM	Data Processor Set AN/TYQ-36(V)1
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
ASYNCH	Asynchronous
ATE	Automatic Test Equipment
ATLAS	Automatic Test Language for All Systems
BiCMOS	Bipolar Complementary Metal Oxide Semiconductors
b/s	Bits per Second
BPSK	Bi-Phase Shift Keying
CAD	Computer Aided Diagnostics
CASS	Consolidated Automatic Support System
CCSK	Cyclic Code Shift Keyed
CD	Compact Disk (Player)
CIIL	Computer Interface Intermediate Language
CMOS	Complementary Metal Oxide Semiconductors
CNCE	Communications Nodal Control Element
Co.	Company
Corp	Corporation
CPU	Central Processor Unit
CRT	Cathode Ray Tube
CSCI	Computer Software Configuration Item
CW	Continuous Waves
D/A	Digital-to-Analog
DAMA	Device Under Test/ATE Matching Algorithm
DARPA	Defense Advanced Research Project Agency
dB	Decibels
dBm	Decibel Above (or Below) 1 Milliwatt
DC	Direct Current
DCL	Diode-Coupled Logic
DIF	Differential Mode Logic
DIP	Dual In-Line Package
DRAM	Dynamic Random Access Memory
DoD	Department of Defense
DOS	Disk Operating System
DSB	Double Sideband
DSP	Digital Signal Processor
DTIC	Defense Technical Information Center
DTL	Diode-Transistor Logic
DUT	Device Under Test
DWG	Digital Word Generator

ECL	Emitter-Coupled Logic
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronics Industries Association
EMI/RFI	Electromagnetic Interference/Radio Frequency Interference
EPROM	Electrically Programmable Read Only Memory
ETR	Effective Test Rate
EW	Electronic Warfare
FACT	Fairchild Advanced CMOS Technology
FAST	Fairchild Advanced Schottky Technology
FET	Field-Effect Transistor
FFT	Fast Fourier Transform
FLIR	Forward Looking Infrared
FM	Frequency Modulation
Freq.	Frequency
FSIC	Communications Control Set AN/TYQ-40(V)
FSK	Frequency Shift Keying
F/T	Frequency or Time
GaAs	Gallium - Arsenide
Gbytes	Gigabytes
Gb/s	Gigabits-Per-Second
GHz	Gigahertz
GPIB	General Purpose Interface Bus
GPS	Global Positioning System
GSI	Grand Scale Integration
HTL	Hybrid-Transistor Logic
Hz	Hertz
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IFF	Identification Friend or Foe
IFTE	Integrated Family of Test Equipment
IMPATT	IMPact Avalanche Transit Time
Inc	Incorporated
I/O	Input/Output
ISDN	Integrated Services Digital Network
ISL	Integrated Schottky Logic
ITA	Interface Test Adaptor
JSTARS	Joint Surveillance and Targeting Attack Radar System
JTIDS	Joint Tactical Information Distribution System
k	Kilo or Thousand
kBits	Kilobits
kBytes	Kilobytes
kHz	Kilohertz
LAN	Local Area Network

LANTIRN	Low-Altitude Navigation and Targeting Infrared System for Night
LS	Low Power Schottky
LSB	Lower Sideband
LSI	Large Scale Integration
M	Mega or Million
mA	Milli-Ampere
MATE	Modular Automatic Test Equipment
Max.	Maximum
Mbytes	Megabytes
Mb/s	Megabits-per-Second
Mem.	Memory
MHz	Megahertz
MIL-STD	Military Standard
MIMIC	Monolithic and Millimeter Wave Integrated Circuit
MIPS	Million Instructions per Second
MMIC	Millimeter Wave Monolithic Integrated Circuit
MOhms	Mega-Ohms
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MRT	Miniature Receive Terminal
ms	Millisecond
MSI	Medium Scale Integration
MSK	Minimum Shift Keying
MUG	MATE User's Group
mW	Milli-Watts
MWords	Megawords
NESEC	Naval Electronic Systems Engineering Center
NIST	National Institute of Standards and Technology
nm	Nanometer
NMOS	N-Type Metal Oxide Semiconductor
NR	Non Return
ns	Nanosecond
NTSC	National Television System Committee
nW	Nanowatt
OP AMP	Operational Amplifier
p-p	Peak to Peak
p/s	Picoseconds
PAL	Programmable Array Logic
PAWS	Computer Graphics Workstation AN/TYQ-37(V)
PCB	Printed Circuit Board
PN	Positive-Negative (Semiconductor Junction)
PROM	
QPSK	Quadrature Phase Shift Keying
R&D	Research and Development
R-Y/B-Y	Red-Yellow/Blue-Yellow
R0	Return to Zero

RI	Return to One
RADC	Rome Air Development Center (now called Rome Laboratory)
Rads	Radians
RAM	Random Access Memory
RC	Return to Complement
Ref.	Reference
Res.	Resolution
RF	Radio Frequency
RFP	Radio Frequency Power
RFV	Radio Frequency Voltage
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RL	Rome Laboratory
RLC	Resistance-Inductance-Capacitance
RMS	Root Mean Square
ROM	Read-Only Memory
RPM	Revolutions Per Minute
RS	Recommended Standard
RTL	Resistor-Transistor Logic
RZ	Return to Hi-Z
s	Second
SAW	Surface Acoustic Wave
SCM	Suppressed Carrier Mode
SCSI	Small Computer System Interface
SECAM	Sequential Color and Memory
Sec.	Second
Seg.	Segment
SOW	Statement of Work
SPECAN	Spectrum Analysis
SPM	Software Programmer's Manual
SSB	Single Sideband
SSI	Small Scale Integration
STC	Schottky Transistor Logic
SVHS	Super Video Home System
T/R	Transmitter/Receiver
TRD	Test Requirements Document
TTL	Transistor-Transistor Logic
TWT	Travelling Wave Tube
ULSI	Ultra Large Scale Integration
μm	Micrometer
μs	Microsecond
USB	Upper Sideband
UUT	Unit Under Test
μW	Microwatt
V/s	Volts-per-Second
V	Volts
Vac	Volts Alternating Current
VCC	VHSIC Central Computer

Vdc	Volts Direct Current
VDP	Video Disk Player
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration
VME	Versa Module Eurobus
Vp-p	Peak-to-Peak Volts
Vrms	Volts Root-Mean-Square
VSWR	Voltage Standing Wave Ratio
VXI	VMEbus Extension for Instrumentation
W	Watts
WAVAN	Waveform Analysis
WORM	Write Once/Read Many
YAG	Yttrium Aluminum Garnet
Z	Impedance